IN THE CLAIMS

Please add claims 32 and 33.

Please amend claim 14 as follows:

1.–13. (Cancelled)

14. (Currently Amended) A method of fabricating a substantially zero signal degradation electrical connection on a printed circuit board, the method comprising:

providing a printed circuit board defined by a dielectric structure core having a first surface, the first surface including a first conducting pad having ~~an~~ a first edge and a second conducting pad having ~~an~~ a second edge separated from and ~~adjacent to~~adjoining the first edge of the first conducting pad, the adjoining edges of the first and second conducting pads defining therebetween a surface area of the first surface; and

applying a solder paste on the first and second conducting pads and on the first surface of the dielectric structure core, the solder paste forming a solder bridge extending between the adjoining edges of the first and second conducting pads that cover~~covering~~ less than an entirety of the surface area ~~of the first surface~~ between the adjoining edges of the first and second conducting pads to form a substantially zero signal degradation electrical connection between the first and second conducting pads.

15. (Previously Presented) The method of claim 14, and further including:

performing reflow soldering of the solder paste applied to the first and second conducting pads and the surface area of the first surface of the dielectric structure core.

16. (Previously Presented) The method of claim 14 wherein applying the solder paste includes:

placing a stencil on the first surface of the dielectric structure core, the stencil defining a first opening sized to substantially correspond to the first conducting pad, a second opening sized to substantially correspond to the second conducting pad and a third opening that links the first opening to the second opening and is sized to correspond to a partial portion of the surface area of the first surface between the edges of the first and second conducting pads; and

applying the solder paste onto the stencil so that the solder paste flows through the first, second and third openings and onto the first and second conducting pads and the first surface of the dielectric structure core.

17. (Previously Presented) The method of claim 16, and further including:

removing the stencil from the first surface of the dielectric structure core; and

performing reflow soldering of the solder paste applied to the first and second conducting pads and the surface area of the first surface of the dielectric structure core.

18. (Previously Presented) The method of claim 14 wherein applying the solder paste includes:

applying the solder paste on the first surface of the dielectric structure core such that the solder paste covers less than 360 square mils. of the surface area of the first surface between the edges of the first and second conducting pads to form a substantially zero signal degradation electrical connection between the first and second conducting pads.

19. (Previously Presented) The method of claim 18 wherein applying the solder paste includes:

placing a stencil on the first surface of the dielectric structure core, the stencil defining an opening sized to substantially correspond to the first conducting pad, the second conducting pad and a portion of the surface area of the first surface between the edges of the first and second conducting pads; and

applying the solder paste onto the stencil so that the solder paste flows through the opening and onto the first and second conducting pads and the first surface of the dielectric structure core.

20. (Previously Presented) The method of claim 19, and further including:
removing the stencil from the first surface of the dielectric structure core; and
performing reflow soldering of the solder paste applied to the first and second conducting pads and the surface area of the first surface of the dielectric structure core.

21. (Previously Presented) The method of claim 19 wherein the stencil includes a plurality of openings in addition to the opening, and wherein prior to placing the stencil on the first surface of the dielectric core the method includes:
masking off at least one opening of the plurality of openings such that the solder paste is prevented from flowing through the at least one opening.

22. (Original) The method of claim 14 wherein the edge of the second conducting pad is separated from the edge of the first conducting pad by a pad edge-to-pad edge separation distance of less than 12 mils.

23. (Original) The method of claim 22 wherein the pad edge-to-pad edge separation distance is 8 mils.

24. – 25. (Cancelled)

26. (Previously Presented) The method of claim 14, wherein applying the solder paste includes:
placing a stencil on the first surface of the dielectric structure core, the stencil defining a first opening sized to correspond to a portion of the first conducting pad, a second opening sized to correspond to a portion of the second conducting pad, and a third opening that links the first opening to the second

opening and is sized to correspond to a partial portion of the surface area of the first surface of the dielectric structure core between the edges of the first and second conducting pads; and

applying the solder paste onto the stencil so that the solder paste flows through the first, second, and third openings and onto the portions of the first and second conducting pads and onto the partial a portion of the surface area of the first surface of the dielectric structure core.

27. (Previously Presented) The method of claim 26, and further including:

removing the stencil from the first surface of the dielectric structure core; and

performing reflow soldering of the solder paste applied to the first and second conducting pads and the surface area of the first surface of the dielectric structure core.

28. (Previously Presented) The method of claim 14 wherein applying the soldering paste includes:

placing a stencil on the first surface of the dielectric structure core, the stencil defining an opening sized to correspond to a portion of the first conducting pad, a portion of the second conducting pad and a portion of the surface area of the first surface of the dielectric structure core between the edges of the first and second conducting pads; and

applying the solder paste onto the stencil so that the solder paste flows through the opening and onto portions of the first and second conducting pads and onto the portion of the surface area of the first surface of the dielectric structure core.

29. (Previously Presented) The method of claim 28, and further including:

removing the stencil from the first surface of the dielectric structure core; and

performing reflow soldering of the solder paste applied to the first and second conducting pads and the surface area of the first surface of the dielectric structure core.

30. (Previously Presented) The method of claim 14, wherein the first surface includes a first substantially square conducting pad having an edge and a second conducting pad having an edge separated from and adjacent to the edge of the first conducting pad.

31. (Previously Presented) The method of claim 14, wherein the first surface includes a first substantially square conducting pad having an edge and a second substantially square conducting pad having an edge separated from and adjacent to the edge of the first conducting pad.

32. (New) The method of claim 14, wherein the solder bridge extends between the adjoining edges of the first and second conducting pads, the solder bridge offset relative to a center point of the adjoining edges.

33. (New) The method of claim 14, wherein the solder bridge extends diagonally between the adjoining edges of the first and second conducting pads.